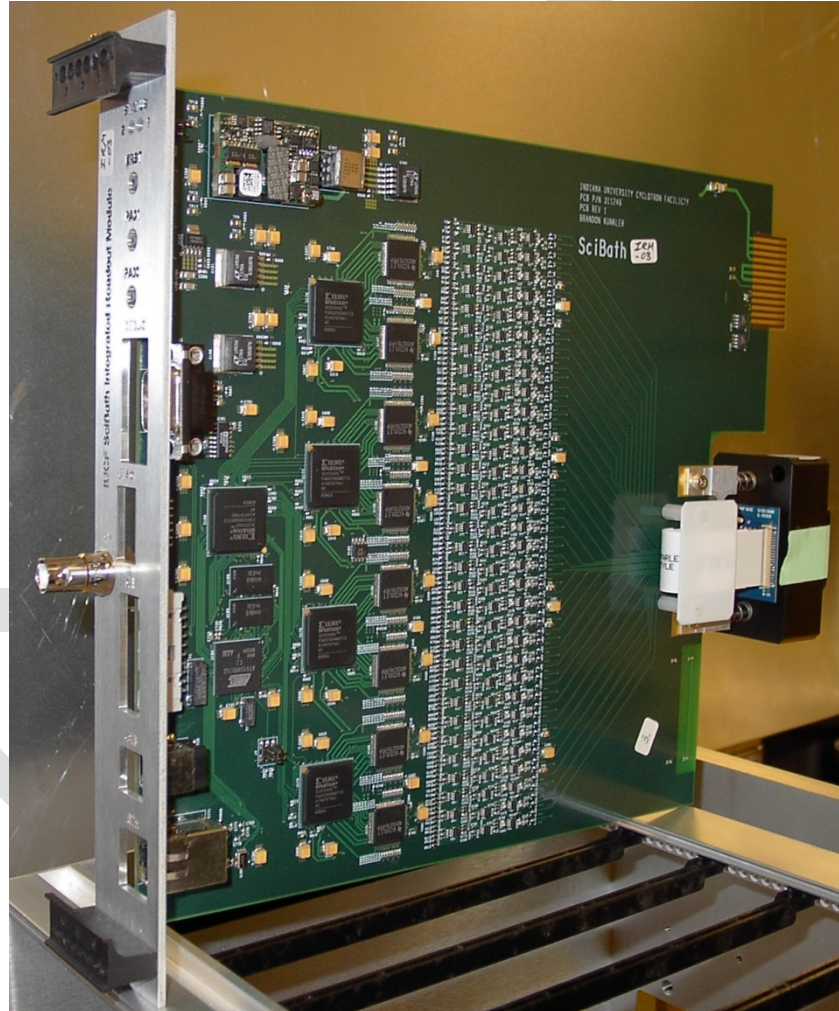




|                 |       |   |      |         |
|-----------------|-------|---|------|---------|
| Document Number | Level | Revision 1  | Page | 1 of 10 |
| Document Title  |       | SciBath Integrated Readout Module Quick Reference |      |         |

IUCF #100003 MS Word Template 10.0

## SciBath Integrated Readout Module Quick Reference





# Indiana University Cyclotron Facility

|   |              |                   |             |         |
|---|--------------|-------------------|-------------|---------|
| <b>Document Number</b>  | <b>Level</b> | <b>Revision 1</b> | <b>Page</b> | 2 of 10 |
| <b>Document Title</b> SciBath Integrated Readout Module Quick Reference |              |                   |             |         |

IUCF #100003 MS Word Template 10.0

## Revision History

| <i>Revision</i> | <i>Effective Date</i> | <i>Purpose of Release</i> | <i>Author</i> | <i>Release By</i> | <i>Release Date</i> |
|-----------------|-----------------------|---------------------------|---------------|-------------------|---------------------|
| 1               | 12/18/2008            | Draft                     | B. Kunkler    |                   |                     |

## Distribution

| <i>Organization</i> | <i>Name or Group</i> | <i>Distribution Method</i> | <i>Date Distributed</i> |
|---------------------|----------------------|----------------------------|-------------------------|
|                     |                      |                            |                         |

DRAFT



|                 |       |   |      |         |
|-----------------|-------|---|------|---------|
| Document Number | Level | Revision 1  | Page | 3 of 10 |
| Document Title  |       | SciBath Integrated Readout Module Quick Reference |      |         |

IUCF #100003 MS Word Template 10.0

## Table of Contents

|       |   |    |
|-------|---|----|
| 1     | Introduction .....  | 4  |
| 1.1   | Purpose.....  | 4  |
| 1.2   | Definitions and Acronyms .....                            | 5  |
| 1.3   | References.....   | 5  |
| 2     | Functional Description .....                              | 6  |
| 2.1   | Pulse Extension .....                                     | 6  |
| 2.2   | Analog to Digital Conversion .....                        | 7  |
| 2.3   | Data Acquisition FPGA (DAQ FPGA).....                     | 7  |
| 2.4   | Processor Interface (Proclf FPGA).....                    | 7  |
| 2.5   | Processor.....  | 8  |
| 2.6   | Debug .....   | 8  |
| 3     | Operating Modes .....                                     | 8  |
| 3.1.1 | <i>Self Trigger Mode</i> .....                            | 8  |
| 3.1.2 | <i>Global Trigger Mode with Zero Suppression</i> .....    | 8  |
| 3.1.3 | <i>Global Trigger Mode without Zero Suppression</i> ..... | 8  |
| 3.1.4 | <i>Charge/Time Summary Mode (Q/T Mode)</i> .....          | 8  |
| 3.1.5 | <i>Raw Data Mode</i> .....                                | 9  |
| 4     | Specifications.....                                       | 10 |
| 4.1   | Electrical .....  | 10 |
| 4.2   | Input/Output.....   | 10 |



IUCF #100003 MS Word Template 10.0

## 1 Introduction

The Integrated Readout Module (IRM) is a 64-channel data acquisition circuit card design for use in the SciBath 300h prototype system [1]. The system consists of a cube containing a matrix of wavelength shifting fibers, an LED calibration system, and 12 IRMs. The system level block diagram is displayed in Figure 1-1.

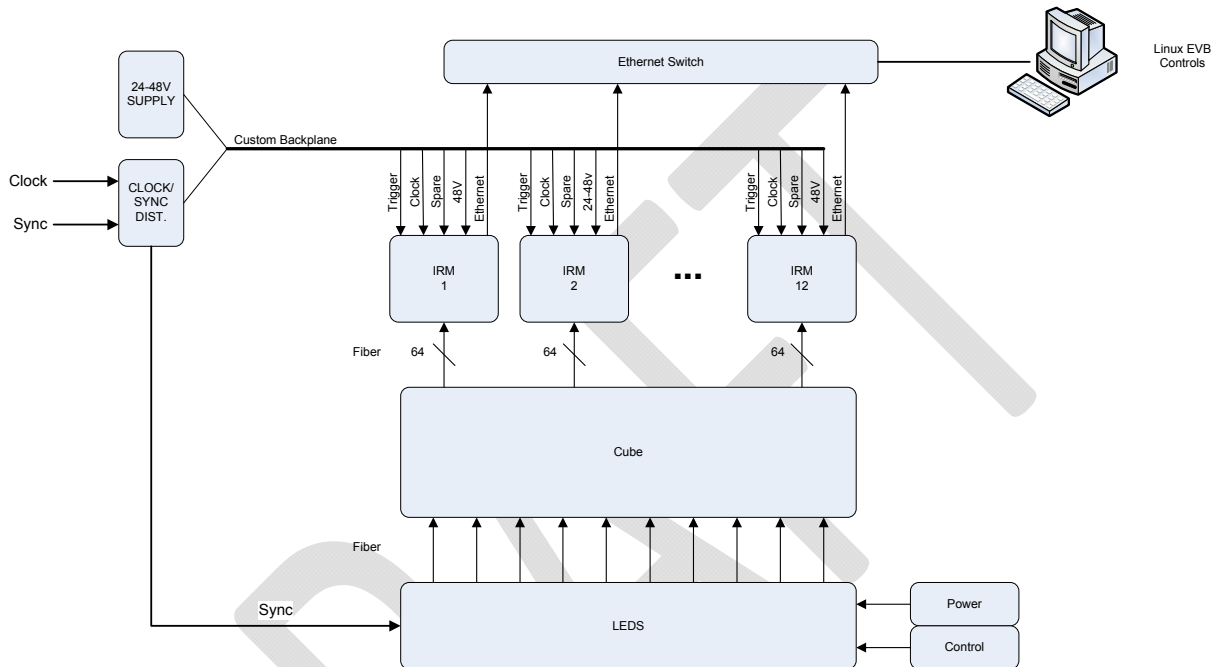


Figure 1-1. System block diagram.

### 1.1 Purpose

The purpose of this document is to provide a high level description of SciBath IRM functionality and to provide basic specifications.



## 1.2 Definitions and Acronyms

| Term | Definition                    |
|------|-------------------------------|
| ADC  | Analog to digital converter   |
| FIFO | First in first out buffer     |
| FPC  | Flex printed circuit          |
| FPGA | Field programmable gate array |
| IRM  | Integrated readout module     |
| PMT  | Photo multiplier tube         |

## 1.3 References

[1] Development of a Novel Neutral Particle Detector, R. Tayloe and H.O. Meyer, November 16, 2005.

([http://www.iucf.indiana.edu/~rex/scibath/docs/FRSP\\_prop.pdf](http://www.iucf.indiana.edu/~rex/scibath/docs/FRSP_prop.pdf))

[2] Performance of Hamamatsu 64-anode photomultipliers for use with wavelength shifting optical fibres, N. Tagg, et al., 2004.

([http://www.iucf.indiana.edu/~rex/scibath/docs/R7600\\_tests\\_oxford.pdf](http://www.iucf.indiana.edu/~rex/scibath/docs/R7600_tests_oxford.pdf))

[3] Development of a Novel Neutron Detector to Measure Ambient Neutron Flux  
H.O. Meyer and R. Tayloe, March 8, 2005.

([http://www.iucf.indiana.edu/~rex/scibath/docs/NNSA\\_technical.pdf](http://www.iucf.indiana.edu/~rex/scibath/docs/NNSA_technical.pdf))



IUCF #100003 MS Word Template 10.0

## 2 Functional Description

The IRM is comprised of a 64-anode PMT, 64 analog channels, five FPGAs, and an ARM processor. The architecture of the module displayed in Figure 2-1. The major functions of the IRM are outlined in the following sections. A description of the inputs and outputs is given in Section 4.2.

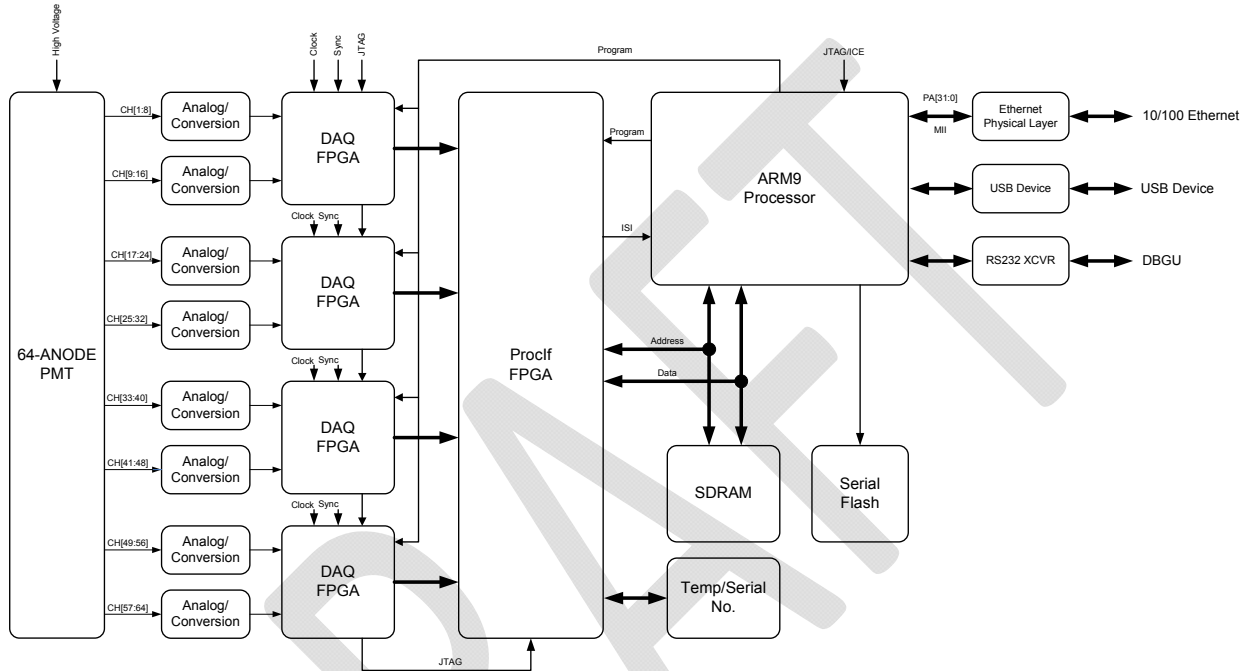


Figure 2-1. Integrated Readout Module architecture.

### 2.1 Pulse Extension

The analog interface to the PMT is a second order active filter. The short PMT pulses approximate a delta function which causes the filter to output its exponentially damped sinusoidal transfer function. This transfer function is much longer than the PMT pulse, allowing the signal to be sampled at a much lower rate than the raw PMT output would require. The filter output in response to a PMT pulse that was captured with the IRM is displayed in Figure 2-2.

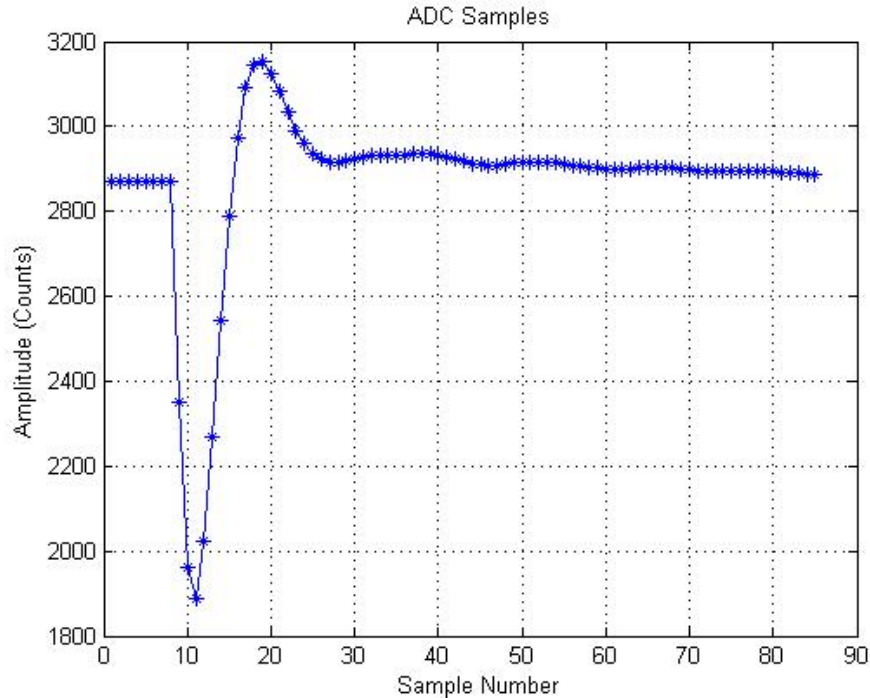


Figure 2-2. Filter response to PMT pulse.

## 2.2 Analog to Digital Conversion

The extended PMT output pulses are sampled by 8-channel ADCs capable of sample rates of 20MSPS to 40MSPS. The ADCs interface to an FPGA that captures their output data.

## 2.3 Data Acquisition FPGA (DAQ FPGA)

The DAQ FPGA provides logic for the ADC interface, the time stamp generator, the threshold detector, and PMT data buffering. Each PMT (ADC) data channel has a buffer implemented using a 1024 deep FIFO. Data is written to the FIFO (captured) when the requirements of the operating mode are met. Data is stored in the buffer until it is requested by the Processor Interface FPGA.

## 2.4 Processor Interface (ProclF FPGA)

The processor Interface (ProclF) FPGA interfaces to the ARM processor and each of the four DAQ FPGAs. The ProclF FPGA appears as a static RAM device to the processor and contains registers for PMT data records, FPGA status, and FPGA control. The PMT data is stored in an 8192 deep FIFO that is accessed through a single address. A finite state machine schedules transmission of data from each DAQ FPGA over a 4-bit interface. Control information is sent to and status data is received from the DAQ FPGA via a separate serial interface.



## 2.5 Processor

The ARM9 processor is responsible for curve fitting and scheduling data for transmission over the 100 base-T Ethernet interface. A USB interface provides support for the download of application images to flash memory. The processor also is responsible for FPGA configuration using files transmitted over Ethernet.

## 2.6 Debug

The IRM has numerous interfaces that are useful for application debug. The processor's serial debug port is connected to a front panel connector. There is a JTAG interface provided for the processor and a JTAG interface provide for the FPGAs, allowing for simultaneous debug of all devices from the front panel.

## 3 Operating Modes

The Integrated Readout Module supports a number of operating modes, making useful for various types of experiments.

### 3.1.1 Self Trigger Mode

Self-trigger mode is useful for experiments where there is no need to synchronize data acquisition with an external event and minimal data rates are required. In this operating mode data is collected when samples have amplitudes greater than a programmable threshold (zero suppression is used). This mode is equivalent to turning off Global Trigger mode.

### 3.1.2 Global Trigger Mode with Zero Suppression

Certain experiments may require samples from every channel be taken only when the signals are non-zero (zero suppression is used) and when an external trigger present. When a trigger occurs and there is no event present, the IRM will not record the sampled data.

### 3.1.3 Global Trigger Mode without Zero Suppression

Some experiments could require samples from every channel be taken, regardless of signal amplitude (no zero suppression), based on an external trigger. The trigger may occur when there is no event present and the electronics will forward the sampled data anyway. The trigger may also be delayed or advanced with respect to an event of interest.

### 3.1.4 Charge/Time Summary Mode (Q/T Mode)

Collecting data continuously during experiments would create the need for high bandwidth interfaces. To reduce the amount of data collected, the charge summary will be calculated and time stamped. Only these values are transmitted from the IRM in this mode. The time stamp



|                 |   |            |      |         |
|-----------------|---|------------|------|---------|
| Document Number | Level   | Revision 1 | Page | 9 of 10 |
| Document Title  | SciBath Integrated Readout Module Quick Reference |            |      |         |

IUCF #100003 MS Word Template 10.0

value is synchronized to the ADC sample clock. Charge-time summary can be operated concurrently with either Global Trigger mode or Self-trigger mode.

### 3.1.5 Raw Data Mode

Raw data mode passes all raw ADC samples without calculating the charge summary. Raw Data mode is equivalent to turning off Q/T mode. Raw Data mode can be operated concurrently with either Global Trigger mode or Self-trigger mode.

DRAFT



## 4 Specifications

### 4.1 Electrical

| Parameter                    | Min | Typ  | Max | Unit |
|------------------------------|-----|------|-----|------|
| <u>Supply Voltage</u>        |     |      |     |      |
| Circuit Card                 | 36  | 48   | 49  | V    |
| PMT                          |     | 800  |     | V    |
| <u>Supply Current</u>        |     |      |     |      |
| Circuit Card                 |     | 0.50 |     | A    |
| PMT                          |     |      |     |      |
| <u>Power Dissipation</u>     |     |      |     |      |
| Circuit Card                 |     | 24   |     | W    |
| PMT                          |     |      |     | W    |
| <u>Operating Temperature</u> | 0   |      | 70  | °C   |

### 4.2 Input/Output

All connections to the IRM are made on the rear 26-pin card edge connect, rear FPC connectors, or front panel connectors.

| Function            | Level/Standard             | Location         |
|---------------------|----------------------------|------------------|
| Circuit Card Supply | Volts DC                   | Rear (Card Edge) |
| Clock Input         | LVDS                       | Rear (Card Edge) |
| Trigger Input 1     | LVDS                       | Rear (Card Edge) |
| Trigger Input 2     | LVDS                       | Rear (Card Edge) |
| PMT Signal          |                            | Rear (FPC)       |
| PMT Supply          | Volts DC                   | Front Panel      |
| Ethernet            | 10/100 Base T              | Front Panel      |
| FPGA JTAG           | IEEE® 1149.1               | Front Panel      |
| ARM JTAG            | IEEE® 1149.1               | Front Panel      |
| ARM ebug            | RS-232                     | Front Panel      |
| USB                 | 2.0 Full Speed<br>(12Mbps) | Front Panel      |